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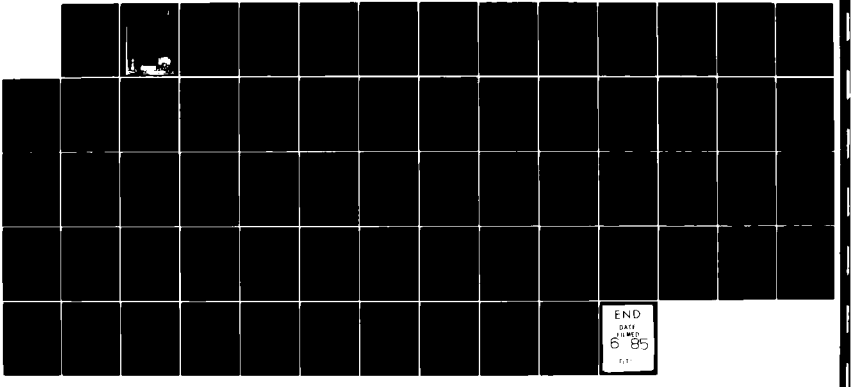

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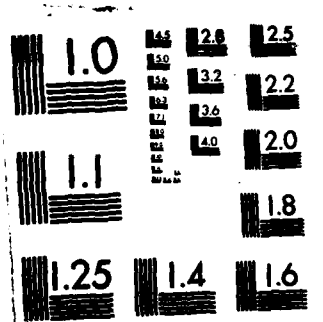

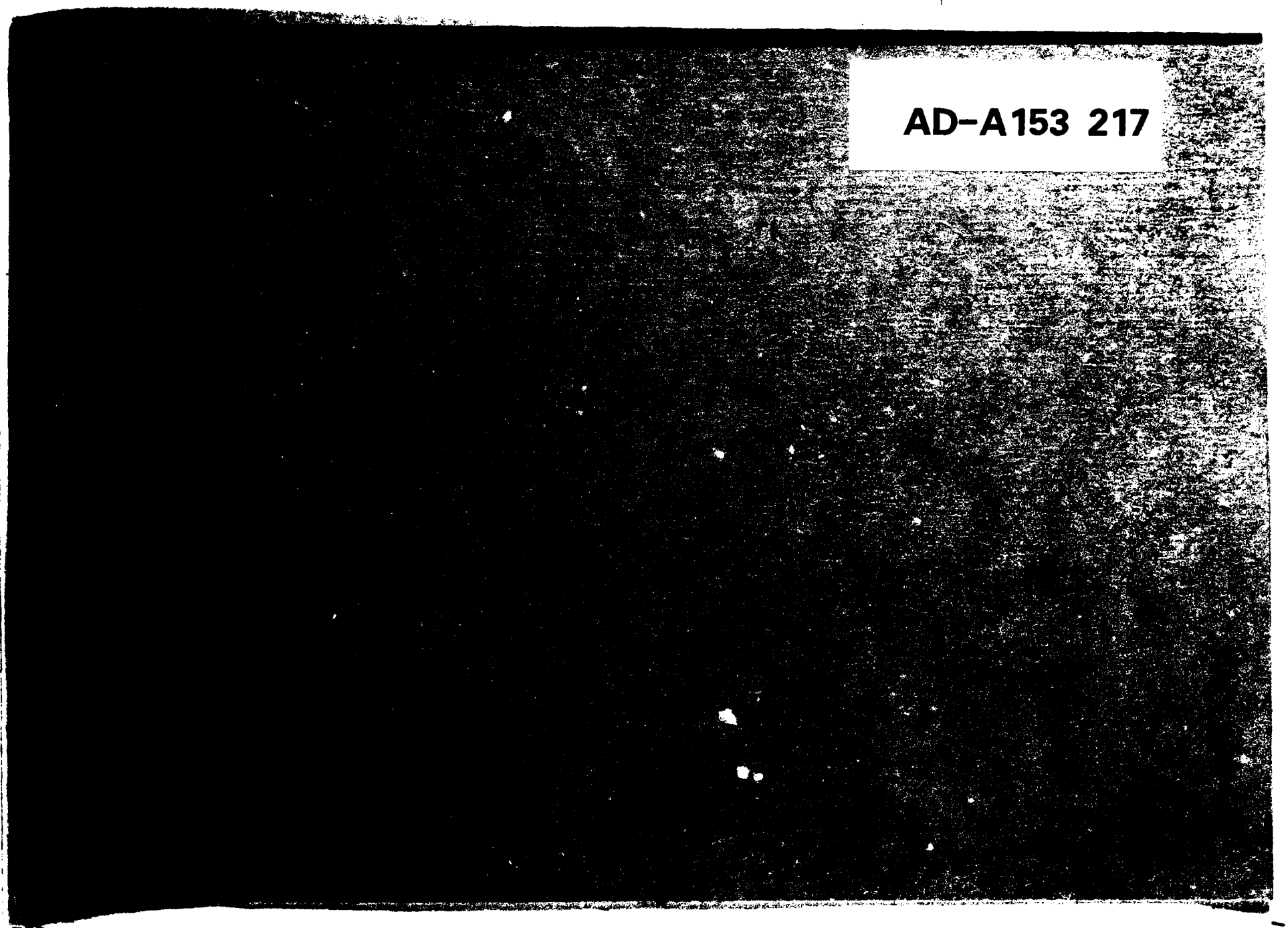
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DOCUMENTATION

ON

ADVANCED RESEARCH

INSTITUTE ON ELECTRONIC MICROSTRUCTURE

MARCH 14, 20 1982

LES DEUX ALPES

I.1. - THE GOAL OF THE CONFERENCE

The general Conference objectives were to assemble an interdisciplinary body of some fifty distinguished scientists and technologists from United States and European countries under the auspices of a NATO Advanced Research Institute to address the issues raised by the recent phenomenal developments in microelectronics. Key questions begin with the choice of materials (Silicon, III-V semiconductors, superconductors), the focussing of imaginative novel concepts, technology (often dictated by materials properties and device requirements), fabrication techniques and instrumentation, and operating environment. These were topics that must be appreciated and understood by a wide audience.

It was felt that this is a crucial time to assemble authorities in the various disciplines in order to focus future efforts into the most productive and effective avenues. In particular, the explosive interest in submicron technology, with its attendant materials, scientific, energy, and strategic overtones, has been the principal topic of discussion. The objective was to understand the present, to be cognisant of the limitations and to propose directions for the future.

I.2. - THE ORGANIZATION

The organization of the Conference has been carried out by a committee of seven persons.

Twenty-five invited papers have been given during the five days of the Conference and have given rise to a lot of interesting discussions. The programme and the list of the participants are given in the last part of the documentation.

At the end of the Conference, three specialized workshops have been organized.

.../...

II - THE MAIN TOPICS OF THE CONFERENCE

The main fields of the Conference were related to the following points :

- semi-conductor materials : elaborating methods, electronic properties,
- devices technology,
- device physics (particularly concerning submicronic devices),
- V.L.S.I.,
- commercial market discussions.

In addition, three workshops have been organized on the following topics :

- microelectronic teaching in European countries and in the United States.
- the future : biolectronic
- carrier transport in submicronic devices.

In addition , a lecture has been given on the microelectronics in China.

III - THE MAIN RESULTS

The most interesting points appear to be the following :

III.1. - MATERIALS

If GaAs remains the most interesting III V materials, devices realized by using the heteroepilayers (Ga Al As / Ga As or Ga In As P / In P) will be more used in the future, not only for optoelectronics but for digital and analogic applications.

However, it should be pointed out that impressive performance can also be obtained by using submicronic Si MOSFET.

.../...

III.2. - TECHNOLOGY

Considerable improvements have occured during the three last years. A lot of new process have been proposed (such as localized epilayers) but the usefulless of such process for practical device has to be proven.

III.3. - DEVICES

Physic - Due to non steady state carrier transport, it shcould be possible to achieve in submicronic devices very high drift velocity and consequently to realize very fast devices. However, two main problems occur :

- how to achieve the experimental check of all the phenomena which occur.
- how to reduce parasitics which in submicronic devices are very important.

Devices - The future of Josephson devices is not clear, taking into account the high level of performance achieved by III V semi-conductor devices at room and at nitrogen temperature.
Acoustic devices appear to be a very interesting alternative in many cases of signal processing.

III.4. - III V DEVICES VERSUS Si DEVICES

In the near future, the commercial market of III V will be always a very small part of Si market. To increase the III V market, new fields of application of microelectronic have to be found.

IV - CONCLUSION

The main goals of the Conference have been reached. The main interests have been to have succeeded to get together at full time during five days, many authorities in the various disciplines of the microelectronics. A lot of very usefull information on the future have been obtained during the presentation of the papers and during all the discussions.

ORGANIZING COMMITTEE FOR NATO ARI ON

"MICROELECTRONICS - STRUCTURE AND COMPLEXITY"

March 1982 - Les Deux Alpes, France

Dr. R. Dingle	Bell Laboratories 600 Mountain Avenue Murray Hill, New Jersey 07974 U.S.A.
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THE PROGRAMME

NATO-ARI

Microelectronics

Les deux Alpes

France

March 14-20, 1982

SPEAKERS		*TITLES*
Barker, J. R.	-	"Complexity Issues - Device-Device Coupling on a Chip" *New Modes of Operation*
Borel, J.	-	"Device and Circuit Physics Today" *The 1.0 μm Barrier*
Bowden, M.	-	"Resists - Today and Tomorrow"
Broers, A. N.	-	"Fundamental Limits to Microfabrication" *Tools, Materials, Resists and Processing*
Carter, F. L.	-	"Toward Computing at the Molecular Level"
Constant, E.	-	"Specific Features of Carrier Transport in Submicron Devices" *What Improvement in Performance Can Be Expected?*
Dingle, R.	-	"The Strange Story of the Superlattice"
Eastman, L. F.	-	"Structures and Phenomena for High Velocity Electrons and High Speed Transistors"
Engl, W.	-	"Self-Test and Reconfiguration of Integrated Systems" *Self Testing, Self Regulating, Self Organizing*
Fichtner, W.	-	"Devices at the 0.1 μm Frontier" *The Silicon-Oriented Story*
Jutzi, W.	-	"Superconducting Devices - Josephson Junctions"
Kimerling, L. C.	-	"Silicon: Past, Present and Future"
Lehmann, H. W.	-	"Etching Techniques"
Maersheld, J.	-	"Analog-Digital Signal Processing"

Magershak, J. - "Circuit Fundamentals"
Operation of Building Blocks and Functional Analog and Digital Cells

McAlear, J. H. - "Bioconductors - Beyond VLSI"

Nicolis, J. S. - "The Role of Chaos in Reliable Information Processing"

Noblanc, J-P. - "Hybrid Circuits - Optoelectronics"

Nuzillat, G. - "Devices and Circuits at 0.5 μm"
The GaAs - Oriented Story

Osgood, R. M. - "Laser Direct-Writing for Repair and Correction on Chip"

Rapp, P. E. - "Chaotic Behavior in Neurons"

Roberts, K. V. - "Construction and Documentation of Software"

Smith, H. - "New Approaches to Single-Crystal Thin Films for Device and Systems Using Surface Patterns"

and

"Report on MIT - VLSI Meeting - January 25-27, 1982"

Sumney, L. W. - "VHSIC Status Report 1982"

Wood, C. E. C. - "Evolution in Trends for MBE Materials and Devices"

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	
CHAIRMAN:	R. Dingle	H. Wittmann	H. Friedrich	B. Wilson	J. Barker
8:00	A. Broers	M. Bowden	H. W. Lehmann	Dr. Noblanc	F. Carter
9:00	L. Kimerling	E. Constant	L. Sumney	H. Smith - MIT VLSI	P. Rapp
10:00	H. Smith	Intro VLSI	J. R. Barker	J. Maerfeld	J. Nicolis
11:00				FREE	Work Shop
12:30				FREE	Lunch
2:00				FREE	Work Shop
3:00				FREE	Work Shop
CHAIRMAN:	H. Queisser	G. Miller	H. Smith	FREE	
4:00	J. Borel	W. Fichtner	W. Engl	FREE	4:00 - Break 4:30 - Conclusions Directions Achievements
5:00	W. Jutzi	R. Dingle N. Linh	R. Osgood K. Roberts	FREE	
6:00	BREAK	BREAK	BREAK	FREE	
6:30	C. Wood	G. Nuzillat [J. Magershak]	Work Shop	Cocktails	
7:00	L. Eastman	J. McAlear			

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ABSTRACTS

FUNDAMENTAL LIMITS TO MICROFABRICATION– TOOLS, MATERIALS, RESISTS AND PROCESSING

by

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ABSTRACT

This talk will review the fundamentals of microfabrication tools and processes. Optical, X-ray, electron and ion beam methods will be compared in terms of both their realistic production capabilities and their ultimate limits. Resists and etching techniques will be similarly compared.

SILICON: PAST, PRESENT AND FUTURE

by

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ABSTRACT

The thrust of silicon materials research and development has been evolutionary and naturally fed into future needs. As device function has become more sophisticated, higher tolerances in materials properties have been demanded. As device fabrication has become more complex, the interactions among the rapidly increasing numbers of processing steps have become a dominant concern. Thus, device technology has developed by an iterative process of modification of design and standard processing. This traditional path of progress is expected to end when device dimensions approach 2 μm in size and fundamental changes in existing processes will have to be introduced.

As device dimensions shrink, materials processing temperatures must decrease to maintain geometric stability. This new era of low temperature processing must feature the introduction of new methods as well as the scaling down of conventional procedures. The projected roles of plasma deposition, pulse heating, and high pressure oxidation will be considered in the light of this interaction with conventional processes. The compatibility of an all low temperature processing scheme will be assessed with respect to the competing requirements of dopant diffusion, defect and impurity gettering, and passivation and isolation structures.

Innovations in device design and function will introduce new frontiers in silicon materials science. The relevant properties will no longer reflect a bulk average, but rather a local volume. The roles of hitherto uninvestigated phenomena, such as local strain fields, on the uniformity of performance must be understood. Smaller devices will introduce larger electric fields during operation. The interaction of the fields with previously tolerated imperfections must be assessed.

Future directions in silicon technology will be projected, and intrinsic limitations of the silicon materials system will be outlined.

New Approaches to Single-Crystal Thin Films

For Devices and Systems Using Surface Patterns*

by

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ABSTRACT

Electronic, optical and surface-acoustic-wave devices utilize only a thin surface region of the single crystal substrates in which they are formed. Substantial improvements in integration and performance could be achieved if appropriate single-crystal materials could be prepared in thin-film form on optimized substrates, and if several materials could be integrated on the same substrate. Current materials growth techniques severely limit the number of film/substrate combinations available for device fabrication. Two techniques currently being developed, graphoepitaxy and zone-melting recrystallization with planar fabricated patterns, promise greater flexibility in combining films with substrates, and could lead to greatly increased integration of devices. In graphoepitaxy, a surface pattern is used to manipulate and control (i.e., to engineer) one or more of the phenomena operative in film formation: nucleation, growth coalescence, reorientation. Typically, a submicrometer-period surface relief structure, having a predetermined two-dimensional symmetry, is used as a template to achieve an oriented film. Thus, graphoepitaxy combines microfabrication and crystal growth techniques. Research on graphoepitaxy is still at a relatively early stage. The validity of the approach has been established, but considerable basic research needs to be done on microfabrication, as well as growth processes, before we can realize its full potential to improve crystalline film quality and expand the number of film/substrate combinations. Zone-melting recrystallization, originated in the 1950's, has seen a rebirth with laser, electron beam and strip-heater recrystallization. Si films recrystallized with a strip-heater have shown surface mobilities for majority carriers comparable to bulk mobilities and superior to SOS. Ordinarily, a film consists of approximately parallel grains with (100) texture. However, grain boundaries and subboundaries can be manipulated by means of surface pattern fabricated by planar techniques. For example, if the molten zone is scanned through a planar constriction a single grain orientation can be selected. The zone-melting recrystalline techniques can also be applied to III-V and other compound semiconductors, and this could lead to a significant increase in the number of film/substrate combinations available and to new capabilities in integration.

* This work was sponsored by the Joint Services Electronics Program, the Defense Advanced Research Projects Agency and the Naval Ocean Systems Center.

Superconducting Devices - Josephson Junctions

by

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ABSTRACT

One of the major vehicles for miniaturization is the semiconductor field effect transistor technology. The usual scaling laws predict a power density and line delay to be independent of the scaling factor. For true scaling of the subthreshold leakage current the temperature must be reduced. Even in this case the delay of open ended normally conducting transmission lines will finally dominate the logic delay since the device switching times are scaled down. Superconducting transmission lines, however, matched with their characteristic impedances, yield minimum lines delays given by the velocity of a TEM-wave, even at submicron cross sections. The current density in submicron cross sections can probably be much higher in superconductors than in normal conductors without electromigration effects. Josephson junctions are promising devices to work with superconducting lines since their power delay time product is in the aWs-range and their load impedances are sufficiently small to match characteristic impedances of feasible strip lines.

Scaling laws of Josephson interferometer circuits are discussed down to minimum line widths of 0.2 μm. Potential advantages of Josephson Junctions with native tunnel oxides or other spacers are briefly reviewed. Mainly the lead alloy and niobium technologies are discussed. For VLSI, the importance of fabrication tolerances of digital circuits with tunnel current threshold devices is emphasized.

EVOLUTION AND TRENDS FOR M.B.E. MATERIALS AND DEVICES

by

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ABSTRACT

The control of independent growth parameters and real-time surface analysis available with M.B.E. has allowed unprecedented progress in both understanding and progress of many metal, semiconductor and insulator auto- and hetero-epitaxial systems. Such is the power of this technique that uniformities and reproducibilities of layer structures and abruptness of carrier profiles and heterojunction interfaces, allow conventional devices to be improved significantly.

More interestingly, doped and composition profile control with angstrom resolutions is now a driving force for the investigation of and realization of completely new devices in new and existing material systems.

This paper discusses some of the more interesting developments in III-V, IV and II-VI materials and devices, and gives subjective predictions of future trends and limitations of this exciting technique.

STRUCTURES AND PHENOMENA FOR HIGH VELOCITY ELECTRONS AND HIGH SPEED TRANSISTORS

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ABSTRACT

Means of obtaining high average electron velocity in thin layers of GaAs and related compounds are covered. Electron energy must be limited to less than .34 eV. In the 100 crystal direction, the maximum group velocity is 1×10^8 cm/S. During gradual acceleration in this direction over distances at or below electron velocity values at or just above 4×10^7 cm/S, but below 5×10^7 cm/S, are possible. The electron mean free path length ranges from .1-.15 μm for electron energy between .08 and .34 eV. At the higher energy the average scattering angle is about 7.5°, while it is about four times larger at the lower energy. Thus a few collisions, launching .036 eV polar optical phonons, are possible and they still allow high average velocities. Acceleration in short distances, $<$ .05 μm, to a desired electron energy less than .34 eV, allows longer drift distances at higher velocity. Average drift velocity at or above 8×10^7 cm/S is then possible over distances at or below .4 μm. Molecular beam epitaxy and fine line lithography make four types of ballistic-electron transistors possible with less than one picosecond transit time using these phenomena. These devices will be described. One is the usual FET with .14 μm gate length and .4 μm source-drain spacing. Another is the permeable base transistor with .4 μm separation of anode and cathode N^+ contact layers. Another is a ballistic unipolar n-type transistor with barriers between emitter and base, and between base and collector. Either a planar doped barrier or a heterojunction potential discontinuity can be used to launch the ballistic electrons into the base. The final version is the ballistic heterojunction bipolar transistor. The average electron velocity in the short barriers is about 4×10^7 cm/S, while the average electron velocity in the base is about $8-9\times10^7$ cm/S.

Such very high electron velocity values compare favorably with the 3×10^7 cm/S average electron velocity in longer modulation doped heterostructures at 77°K. These velocity values all allow proportional rises in the g_m/C values for the transistors, which in turn allow higher frequency response and higher switching speeds.

RESISTS TODAY AND TOMORROW

by

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ABSTRACT

Microcircuit fabrication requires the selective diffusion of tiny amounts of impurities into specific regions of a semiconductor substrate (e.g., silicon) to produce the desired electrical characteristics of the circuit. These regions are defined by lithographic processes in which the desired pattern is first defined in a resist layer (usually a polymeric film which is spin coated onto the substrate) and then transferred via processes such as etching to the underlying substrate. There are a number of lithographic techniques either in use or currently being evaluated. These include photolithography (including its extension to the so-called deep UV region, viz., 2,000-3,000A), electron-beam lithography, x-ray lithography and ion-beam lithography. Each of the technologies involves the common feature of causing chemical changes in the resist system which enable the exposed regions to be differentiated from the unexposed regions by solubility differences or differences in plasma etch rate thereby forming a three dimensional relief image of the circuit pattern in the resist. Resist materials must be designed to respond to the particular form of exposing radiation, viz., UV light, electrons, x-rays or ion beams. This requires a fundamental understanding of the interaction between radiation and matter and of the various material and exposure parameters which determine lithographic performance. Following a brief review of the fundamental aspects of resist exposure, this paper will review specific resist design features pertinent to the different exposure technologies while pointing out the physical and chemical properties of resists which limit resolution. The continuing trend towards smaller and smaller feature sizes is placing ever increasing stringent requirements on resist performance. Several new approaches to resist design and performance have emerged in recent years. These include multilevel schemes, inorganic resists, plasma developable resists and resists incorporating new mechanistic approaches. These areas are seen today to constitute the forefront of research on resists and will be reviewed in this paper.

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Non Steady State Carrier Transport In Submicronic Devices

What Improvement In Performance Can Be Expected

by

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ABSTRACT

The main goal of the microelectronic industry is to make ever increasing numbers of smaller devices on a single chip. In this type of device, carriers are often in non steady state conditions and it is the purpose of this paper to study if the specific features of electron transport in such conditions could be used to greatly increase the velocity of the carrier and to obtain high performance submicronic devices by reducing the transit time of the carrier.

The physical mechanisms determining the velocity of carriers in a semiconductor are first reviewed and it is shown that velocities considerably higher than in steady state can be realized in specific conditions. Assuming a homogeneous field in the semiconductor it is discussed how such conditions can be almost achieved by applying either time step or time pulse configurations of the electric field. In the first case, the electric field is applied throughout the motion of the electrons and overshoot velocity can be observed. In the second case, almost all the motion, after the initial acceleration due to the electric field pulse, is carried out without a driving field and a pure ballistic motion is obtained. In both cases the maximum average velocity which could be achieved for a carrier traveling over a distance d in GaAs is calculated by Monte Carlo methods. The influence of the doping concentration and of the operating temperature, as well as the improvement which could be achieved by using other materials are also discussed.

The potential of such ballistic motion and velocity overshoot in a real submicronic device is then assessed and it is shown that, due to spatial non uniformity, additional phenomena occur which might considerably change and often reduce the velocity of the carriers.

In conclusion taking into account the results obtained we discuss the various ways which could be used to increase carrier velocities in submicronic devices using homo or heteroepilayers.

Devices at the 0.1μm frontier

The silicon-oriented story

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The continuing trend for higher packaging density, higher system speed and increasingly complex circuits has resulted in a drive over the last few years towards reducing the geometrical dimensions of devices. Whereas the linewidth for high-volume production circuits has been reduced form 3.5 μm to less than 2 μm, strong efforts have been undertaken at several industrial laboratories (esp. Bell Labs, IBM, TI) to study the behavior of FETs with gatelengths of 1 μm or less. Circuits have been fabricated whose speed results not only exceed data achieved by conventional bipolar ECL, but seriously challenge III-V materials as the only choices available for high frequency applications.

In this contribution I shall concentrate on the following subjects:

a) Scaling properties of silicon FETs - Theory and Experiments

Recently, we have proposed a generalized guide to FET scaling which is based on a wide range of experimental results and computer simulations. Experimential data have been published on devices with channel lengths as small as 0.1 μm (n-channel) and 0.5 μm (p-channel). We find that the supply voltages have to be reduced in order to avoid excessive leakage due to hot carrier effects (impact ionization, carrier injection into SiO_2). However, conventional planar FETs will still be seriously limited by the parasitic resistance in the external source and drain areas.

b) Technology requirements for submicron-size FETs

Stringent requirements arise for the processing steps necessary to fabricate very small devices. I shall address the necessity of low-temperature processing, the requirements for pattern definition and pattern transfer, the need for multilevel metallization schemes and the importance of improved isolation techniques.

c) High speed silicon circuits and circuit scaling

I shall present recent results on the performance of fine-line MOS circuits, which demonstrate the inherent high speed potential of silicon. Published results include data on ring oscillators, four-stage counters and a 700 transistor MSI circuit.

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THE STRANGE STORY OF THE SUPERLATTICE

by

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ABSTRACT

In the last year or two much interest has developed in the area of semiconductor heterojunction superlattices, especially those composed of the III-V compounds, GaAs and AlGaAs.

This presentation will summarize the short background history of this area and will conclude with an emphasis on the new device characteristics and the potential for their use in high speed circuits and systems. In keeping with the overall philosophy of this meeting, critical questions to do with this approach will be posed and a comparison with some other competing high-speed approaches will be made.

DEVICES AT THE 0.5-0.3 MICRON SCALE -

GaAs ORIENTED SUBMICRON DEVICES AND CIRCUITS

by

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ABSTRACT

The speed-power tradeoff presently achieved by GaAs logic IC's with half micron geometries will be presented taking advantage of performance measurements on fabricated circuits including ring-oscillators, binary frequency dividers, and static random access memories.

Further performance improvement possibilities derived from device scaling down to the 0.1 micron frontier will be discussed under the light of material and fabrication process constraints by taking into consideration some limitations (crosstalk, impedances...) resulting from the layout of realistic circuit examples. Finally, the practical problems of Gigabit Logic circuits utilization (packaging, clock distribution, I/O data stream handling...) will be briefly assessed with a special emphasis placed on the question of serial/parallel approach tradeoffs in digital signal processing.

CIRCUIT CONFIGURATIONS AND LIMITATIONS WITH NEW HIGH-SPEED INTEGRATED CIRCUIT DEVICES

by

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ABSTRACT

A survey will be given of different basic high speed integrated circuit structures using Si, GaAs and ternary compounds.

The state-of-the-art performances of different logic gates will be given and commented (power, delay times, fan out dependence, etc ...) especially for micron and sub-micron device cells.

Basic analogue functions will also be reviewed and discussed; amplifiers, oscillators, mixers, phase shifters, etc ... and a critical appraisal will be attempted of the different approaches.

Finally predictions and a discussion of the limitations will be undertaken in as far as the basic module structure is concerned for increasing speed and reducing power and surface area.

BIOCONDUCTORS - BEYOND VLSI

by

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ABSTRACT

In research supported by the National Science Foundation (Grant No. DAR 8009745), EMV Associates, Inc., in conjunction with J. Hanker at the University of North Carolina, has recently demonstrated a biotechnical approach to the direct micropatterning of a metal.

The process, which utilizes conventional electron beam lithography and ultracytochemical techniques, results in the attachment of the desired microstructure to free amino groups in a protein/resist composite. The feasibility effort, conducted under the referenced NSF grant, resulted in the fabrication of an array of parallel silver lines, each 4 microns in width (see Figures 1 and 2, below). To the knowledge of the authors, this is the first time micropatterning of a metal has been achieved without intermediate masking and etch-back procedures.

Since the biotechnical process may also be used to micropattern other metals, as well as X-ray opaque materials which can be used to form X-ray micromasks, there are direct and immediate applications to VLSI technology. Using available electron-beam writing equipment, line widths in the order of 0.1 to 0.2 micron should be achievable, an order of magnitude reduction from present state-of-the-art capabilities.

Longer-range development of the biotechnical process promises even more significant applications to VLSI. Following concepts described in U.S. Patents #4,103,064 and 4,103,073 (awarded to the authors in 1978), use of an oriented or paracrystalline protein monolayer offers the possibility of still another order of magnitude decrease in element size (to 10 to 20 nanometers). As depicted in Figure 3, a single electron-beam written window in a protein/resist composite utilizing an oriented monolayer would reveal multiple free amino groups, each of which could be the basis of a biotechnical element. Thus, ultimate packing densities would no longer be limited to electron-beam lithography, but rather would be determined by the protein characteristics.

The significance of the oriented monolayer goes beyond increased packing densities. Firstly, various innovative molecular devices, some undoubtedly meritorious, have been proposed (e.g., a March, 1981 Naval Research Laboratory Workshop presented some 25 papers on molecular electron devices and related subjects). The biotechnical process is the first known that offers a means of assembling and testing such devices. Secondly, cimputer modeling of amino group sequences in the paracrystalline protein may ultimately provide information that would allow specific, genetically engineered protein molecules to be subassembled on the protein, produced biological electronic elements classifiable as semiconductors, insulators and *transductors*.

FIGURE CAPTIONS

Figure 1 - SEM micrograph of silver lines attached to synthetic protein micropattern (1000X).

Figure 2 - Silver L_α X-ray intensity map of region shown in Figure 1. Intensities off lines are background

Figure 3 - Model of protein monolayer and basis for an oriented protein/metal subassembly sequence (a,b,c,d,e,f,g). Such a sequence could resemble that occurring naturally on the membrane of living cells. In this case the location of the pattern is determined by the specific areas where active protein sites are exposed by electron beam lithography. Depending upon the subsequent treatment and the nature of the specific protein molecules, a variety of functional elements are possible such as conductors, semiconductors, insulators and transducers or as superlattices.

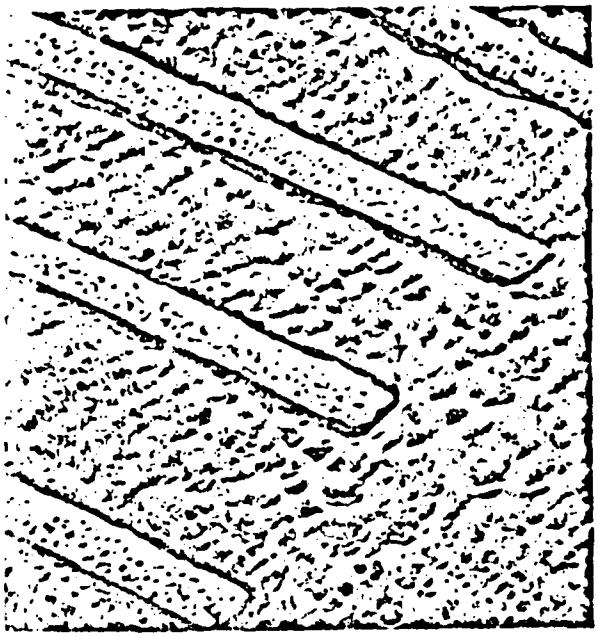

FIGURE 1

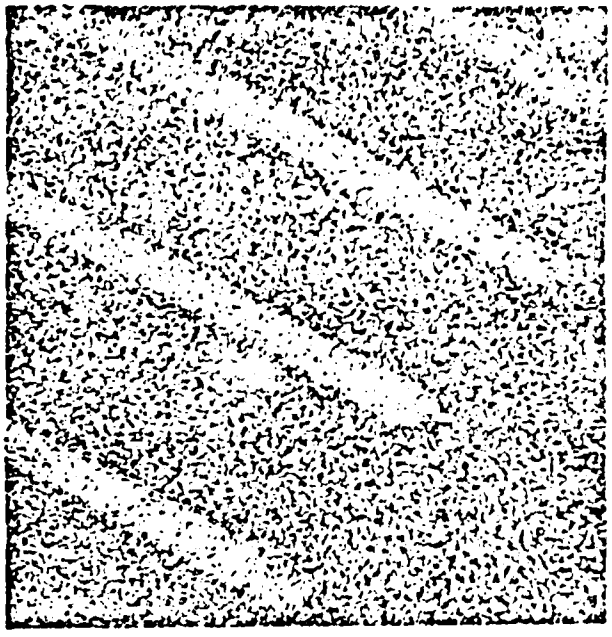

FIGURE 2

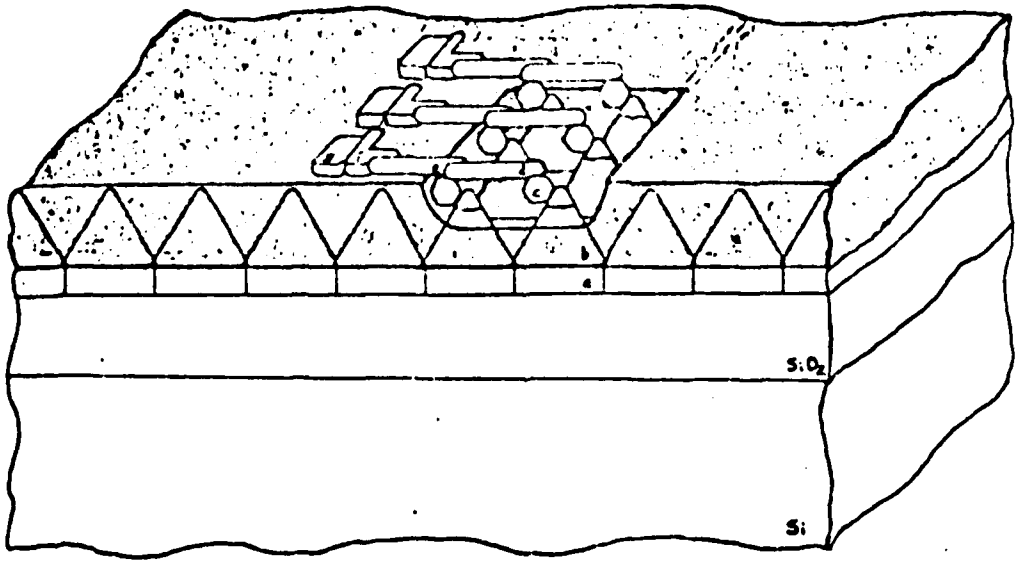

FIGURE 3

ETCHING TECHNIQUES

by

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ABSTRACT

Modern fabrication techniques for microstructures (i.e. VLSI, Josephson Junctions, integrated optics, diffractive optics for visible light or X-rays etc.) require control of linewidths and line spacings in the micron and submicron range. Furthermore, the shape of the line profile has to be well controlled. Whenever such critical dimensional control is required, conventional wet etching techniques can no longer be used for pattern transfer. Although wet etching is usually very selective, it is almost always isotropic, which means that the etch front advances in all directions at the same rate. This makes profile control impossible because of undercutting. One notable exception to this rule is wet etching of single crystal Si which can be highly anisotropic due to the largely varying etch rates for the different crystallographic planes.

In the past few years a number of dry etching or plasma etching techniques have been developed which allow a much better dimensional control in the transfer of fine patterns. The principle in all these techniques (plasma etching in a variety of reactors, reactive sputter etching, reactive ion beam etching or microwave plasma etching) is always the same: A low pressure plasma is produced in a gas, which breaks down into fragments (i.e. !CF sub 4! into F-radicals and !CF sub 3 sup + !-ions) some of which may interact with the sample surface which is immersed in the plasma.

The main advantage of most of these techniques is that etching can be made highly anisotropic which means that structures with large height/width ratio can be mde. The anisotropic nature of etching is thought to be due to the highly directional impact of ions onto the sample surface. This can lead to an ion induced enhancement of the etch rate. Although dry etching of a variety of materials in different gases seems to give empirically similar results in terms of anisotropy and etch rate, the actual etching mechanisms are very different and are presently under investigation in many different laboratories.

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VHSIC Status Report 1982

by

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ABSTRACT

This paper has two purposes. The first is to provide an overall summary of the VHSIC program including rationale, history and objectives. The second is to discuss the current status of its implementation: In particular, the implementation of phase two, the broad participation in the formulation of VHSIC goals and structure, the export aspects resulting from congressionally - mandated imposition of international traffic in arms regulations (ITAR), and the relationship between VHSIC and commercial competition, both domestic and foreign will be described.

COMPLEXITY ISSUES: DEVICE-DEVICE COUPLING ON CHIP

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ABSTRACT

The entry into the VLSI era raises perspective issues which go considerably beyond the *problems of fabrication*, materials control, scaling down individual transistors, circuit performance and so on. Two problems in particular, now appear unavoidable; how to manage the enormous complexity of VLSI systems[1-5] with its potential for massively concurrent computational structures involving distributed processor arrays; and how to overcome the problems presented by the intrinsic unreliability of individual components within an ultra-dense system. In the latter case, it becomes increasingly difficult to insist on the fabrication of a perfect system when we consider the hazards posed by statistical and systematic *fabrication error*, *defect* and fluctuation phenomena, electromigration, hard errors induced by natural radiation. This is particularly true for most present day circuit designs which are vulnerable at the smallest component level - interconnect or transistor. It is also no longer true that the design ideal of producing a distributed array of discrete components - that is totally isolated apart from the connection net - can be maintained as circuit dimensions shrink. Cross-talk effects ranging from simple parasitic capacitive coupling and electromagnetic cross talk between neighboring interconnect/cells to charge spillover, *barrier tunnelling*, thermal crosstalk - all represent perturbative undesigned device-device coupling. Cross-talk is not just a noise problem (although it can be responsible for non-thermal noise or chaos - a feature first realized in the old vacuum-tube universal circuits) but can provide additional parasitic connectivity in the circuit which can switch the intended function of the system and thus appear as a logic error. This is particularly likely in the very regular, highly concurrent architectures proposed in recent years to overcome the design bottleneck afforded by VLSI. Concurrent structures have considerable advantages, particularly hierarchical schemes for programmability, design, system speed, testing, etc.; but involve simultaneous activation of all or most of the circuit elements in the system unlike the older sequential designs. Distributed systems of this kind have analogies in biological media such as the brain, in convection cell structures in fluids, in chemical-reaction kinetics. An essentially common property of dense highly concurrent systems which are subject to either fluctuations, or to nonlinear parasitic device-device or cell-cell interactions, is that they have a propensity to become self-organizing or synergetic. A few collective

modes can undergo destabilizing bi-furcative transitions which lead to new patterns of system operation in response to uncontrolled changes in the system environment. The stability properties of VLSI systems are thus anticipated to be very different from older less complex designs. However, this can be an advantage, it is possible to devise, in principle self organizing structures, either via conventional gates but including variable feedback connection paths, or by exploiting nonlinear device-device coupling in specially configured materials such as the quantum well hetero-structures. The most elementary need for designing self-adapting systems is to resolve the reliability problem - just as the cooperative self organized mode of a laser overrides the frequency fluctuations of individual imperfectly placed atoms in the lamp mode. Progress in this direction, with comments on the implications for the choice of materials configuration including molecular electronics will be reported including a brief description of a hierarchical self organizing system designed for complex control tasks in the presence of uncontrolled time dependent extrinsic and intrinsic system interference. This hardware approach to complex control is briefly compared with the more vulnerable software approach. Finally, we discuss briefly the question of applicability and product innovation for synergetic electronics including perceptual and other artificial intelligence applications.

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SELF-TEST AND RECONFIGURATION OF INTEGRATED SYSTEMS

by

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ABSTRACT

Advantages and attributes of VLSI are welcomed by the user, however, two problems never adequately solved in LSI are getting much worse: determining in a cost-effective way whether a circuit has been manufactured correctly, and providing a high production yield in spite of unevitable failures.

Design For Testability (DFT) is an important tool to solve the first problem. Under the known different DFT techniques the Built-In Test (BIT) seems to be the most effective approach for complex systems because the circuits are testing themselves with only minor external support. Both, test pattern generation and test answer evaluation are done on the chip using functionally converted Linear Feedback Shift Registers (e.g. BILBOS)[1], thus resulting in a minimum overhead. The source of test patterns obtained are pseudorandom number generators and the sink of test answers which have to be compressed are multiple input signature registers. Moreover, the BILBO approach allows to combine BIT and scan techniques.[2] The feasibility of self-testing circuits was demonstrated recently by several devices[3,4].

Partitioning complex circuits into smaller manageable subcircuits is a presupposition not only for self-testing but also for any modern design. A natural outgrowth of this concept promises the solution of the second problem: yield enhancement. In order to tolerate process induced failures, redundant subunits (spare parts) can be placed on chips or even wafers and reconfigured depending on their functionality. Early steps in this direction in the 1960's failed because of discretionary wiring problems[5]. They are now resumed in large memories using irreversible (static) laser programming[6].

Self-testing subunits and dynamic wiring which would offer a more convenient method become possible if a direct writing Electron Beam Pattern Generator (EBPG) is utilized. Depending on self-test results evaluated by the EBPG, the subunits are interconnected and form the final system. In addition, switchable elements for a reversible circuit personalization could be implemented thus finally leading to self-organizing systems.

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LASER DIRECT-WRITING FOR REPAIR AND CORRECTION*

by

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ABSTRACT

The complexity of the metallization patterns on modern microelectronic components such as reticles, ceramic packages and device chips has placed new demands on the development of processing techniques to increase fabrication yields. Further, the manufacture of a small number of such devices is rendered economically impossible. However, the development of techniques to correct, at will, defects in interconnect patterns can relax the requirements on process yield. In some case, the same techniques can be used to facilitate device customization.

The author and his colleagues at M.I.T. Lincoln Laboratory have recently developed several new laser techniques for directly writing and etching metal and semiconductor features on wafers, and quartz or glass substrates. These processes are maskless, requiring only a gas-phase chemical medium and a focussed light beam. Submicrometer resolution has been demonstrated for direct writing of metallization patterns. Repairs on photolithographic reticles have been used to test the technique.

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CONSTRUCTION AND DOCUMENTATION OF SOFTWARE

by

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ABSTRACT

It is well known that software lags a long way behind hardware at the present time and is responsible for a large proportion of the cost, complexity, inefficiency and unreliability of computing. Its intellectual difficulty and lack of standardization make production difficult to control. In this paper some of the basic properties of software including computer languages and programs are examined from first principles and possible solutions put forward.

Software is a class of information that has many analogies with well-established classes such as books and recorded music. These analogies can usefully be exploited and examples are given. There are, however, significant differences. An important feature of present software is that it can readily be duplicated and pirated by straightforward copying so that financing is a problem and it is also readily altered so that it lacks performance and many different versions may exist.

With advances in chip technology it should be practical to combine, on a single package, a processor with sufficient room to contain a substantial program, and to distribute mass-produced execute-only software (EOS) that is built into the hardware and can be used but not readily copied or altered. This might encourage standardization and permanence and make financing more secure.

TOWARD COMPUTING AT THE MOLECULAR LEVEL

by

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ABSTRACT

Signal transport mechanisms operating at the molecular level which might be employed as switching elements has been tabulated in 1979 (1a and 1b). At the same time an outline for the "growth" or chemical fabrication of a computer was given (1a). The most promising opportunities for switching systems at the "molecular" size level involve conformational or structural changes along with charge redistribution. One opportunity involves electron tunnelling in short periodic structures and might be realizable in both layered systems and linear molecular systems. Molecular analogues of conventional NAND and NOR gates will be given. Although soliton propagation in conjugated systems is a relatively slow phenomenon, it offers another excellent opportunity for new approaches. Examples of soliton generation, gang switching, demultiplexing, soliton reversal and a soliton memory element will be given. The density of such switching and memory elements might be at the 10^{18} gates/cc level, assuming 3d construction (2). One of the advantages associated with both electron tunnelling and with soliton propagation is that both phenomena are nondissipative.

The importance of learning to use fabrication techniques involving self-synthesis and self-organization cannot be overstressed. New approaches to material fabrication will be discussed and examples of input output possibilities will be given.

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CHAOTIC NEURAL DYNAMICS: TURBULENT BEHAVIOR IN A BIOPHYSICAL CONTROL SYSTEM

by

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ABSTRACT

The classical view of chemical and biophysical control systems held that a system would necessarily return to its steady state after a displacement. Mathematically, this corresponds to systems governed by fixed point attractors. Subsequent theoretical research demonstrated that thermodynamically open systems far from equilibrium could exhibit periodic motion. This is consistent with the experimentally observed capacity of many classses of neurons to generate sustained nondecaying oscillatory output. Systems displaying rhythmic behavior are said to be governed by periodic attractors.

It has been proposed that there is a third topologically distinct class of dynamical behavior which is fully deterministic in origin but having highly irregular properties. In recognition of the irregularity of these systems, these attractors have been named strange attractors, and the associated output behavior is called chaos. The term chaos is used in this context and more generally to refer to a number of different kinds of complicated behavior. They manifest themselves by giving output which seems to be a periodic and does not approach either a stable oscillation (a periodic attractor) or an equilibrium state (a fixed point attractor). In functional terms the significance of chaotic behavior lies not only in the disordered character of the motion but in the system's extraordinary sensitivity to initial conditions. Trajectories starting arbitrarily close to one another diverge exponentially. This property can be re-expressed in control theory terms by observing that the same system will give very different output even if the input signals are infinitesimally close.

A given system can make transitions between steady state, periodic or chaotic motion as the result of possibly very small changes in the values of internal parameters that are constant under ordinary operating conditions. Examples encountered in neurophysiological contexts would include temperature, ionic composition and the concentration of drugs in the extracellular medium and the value of constant depolarizing currents. A small change in experimental conditions may cause a quiescent neuron to discharge periodically or a change in drug concentration might cause a chaotic neuton to undergo a transition to stable periodic firing.

The motivation for these investigations has three components centered on thermodynamics, neural information processing and clinical defects of neural control. Given the novel character of chaotic behavior, the experimental confirmation of chaotic output from neurons would constitute a major expansion to the class of thermodynamically admissable behavior, and is thus of importance to our understanding of the thermodynamic foundations of biophysics. Similarly, the presence of chaotic neurons raises several important questions about information processing

and control by neural networks. The parameter-dependent transition of normally quiescent or rhythmic neurons to chaotic motion could provide a common mechanism for a number of clinically observed pathologies of neural regulation. Seizure disorders, specifically epilepsy, are obvious candidates. A longstanding view of epilepsy held that the associated neural activity was an ensemble behavior of multi-neuron networks in which an inbalance in excitatory and inhibitory feedback leads to a predominance of excitatory activity. Recent experimental evidence suggests that paroxysmal depolarization results from a presently unexplained active membrane process intrinsic to the cell. A transition to chaotic output could provide both an explanation and a rational for pharmacological intervention. If the parameter displacement causing the dynamic transition can be identified, it may prove possible to design a drug regime specifically directed to resetting that parameter. Analogous arguments can be applied to the study of clinical disorders of movement that have been attributed to defects in central nervous system pacemaker neurons. Examples include Parkinsonian tremor, chorea (a ceaseless occurence of rapid, highly complex, jerky involuntary movements), athetosis (mobile spasm) and dystonia (involuntary, irregular contortions or muscles).

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THE ORIGIN OF CONFLICT IN PHYSICAL AND SYMBOLIC SYSTEMS

by

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ABSTRACT

In this paper we advance the thesis that conflict emerges in two interacting-(Physical) or communicating-(symbolic) dynamical systems as a dilemna of mutually accommodating excessive entropy production. Each system strives towards "Self" - organization at the expense of the partner.

"Self"-organization is meant here to imply the function of a cognitive gadget-"Language"-which compresses the complexity of the "opponent" (environment) thereby providing (proposing) minimal algorithms (programs) which reduce and predict the behavior of the other system.

Usually languages are recursive algorithms. There are cases however, where languages may become involved in circular argumentation - which signals the appearance of paradoxes of self-reference.

Paradoxes emerge whenever the (unsuccessful) attempt to compress the time series received from the environment - and which effort produces excessive entropy production at the hardware level of the system involved - reaches the so-called "Godelian", limit; beyond this limit the incompatibility between completeness and self-consistency in any closed axiomatic (logical) system manifests it self as an inability to discriminate between statements belonging to different hierarchical levels.

When paradoxes flare up within a language-possessing system conflict sharpens; to the previous intersystemic conflict we now witness an hierarchically underlying intra - systemic conflict. Intersystemic conflict resolution depends now on the parameters determining the intra - systemic conflict. This latter in turn uses the intersystemic communication as an expendable device for advancing its own resolution.

The coupling and dynamic evolution of the pair of inter- and intra-systemic conflict will be the theme of the present paper.

The hierarchical systems we are delaing with possess Complexity and Organization. We define complexity as the minimum number of bits required to reproduce a given system. We define organization as the ability to compress information - which in turn is generated via cascading bifurcations giving rise to broken symmetry.

In any game, each participant aims at "breaking" the code of the opponent i.e. "compressing" as much as possible the description of the partner. Achieving compressibility (or cognition) is therefore tantamount of forming collective properties out of the variables of the sytem under study, or, in the domain of a description governed by the solution of the master equation, compressing the p.d.f. to achieve the "mean" field regime.

The origin of conflict can be boiled down to the incompatibility between "compressibility" and intermittency": When the p.d.f. cannot be compressed beyond a certain threshold and "explodes" - intermittency - the mean field approach breaks down and the macrosystem becomes "turbulent" in the sense that it acquires as many degrees of freedom as the microsystem (one hierarchical level below).

This is what we mean by saying that beyond this "Godelian" limit the dynamics on two successive hierarcical levels get "mixed up". Microscopic and Macroscopic description become indistinguishable in the sense that random noise and chaos are statistically similar.

COMMUNICATION BETWEEN TWO HIERARCHICAL SYSTEMS

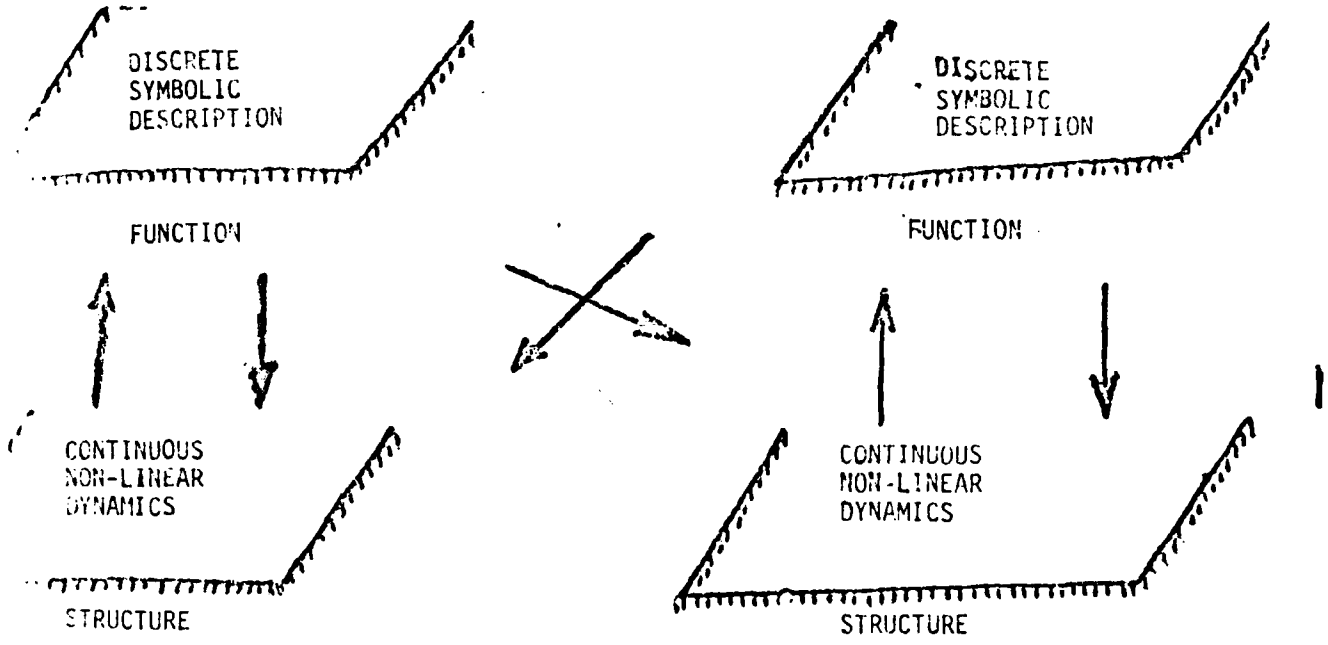

Figure 1

Sketch of two communicating hierarchical systems.

In many cases hierarchical systems are "almost decomposable" in the sense that one can study the dynamical ongoings at a given level taking what is just underneath as a boundary condition and what takes place above as a constant. This can be done whenever the rate constants differ by orders of magnitude from level to level. In linguistic systems this decoupling of levels cannot be accomplished, due to the existance of evolutionary feed forward loops mediating the dynamics between energetic (structural) and symbolic (functional) levels. Specifically in linguistic systems one makes use at the same time of two hierarchical levels where statements and metastatements are interlocked.

Development of Microelectronics in China
— a review

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Beijing, China 1982

Development of Microelectronics in China — a review

With the increasing importance of microelectronics in national economy and science technology, research and development in this field carried out by China's science and production units are accordingly developing in depth and width.

This paper will review the present status of China's LSI, microfabrication technology and some R & D work done in the area of IC.

I Present Status of LSI in China

Line width of N channel silicon gate devices are decreasing from 6～7μm to 3~4μm level. Multilayer Poly-Silicon, multi ion implantation particularly arsenic ion implantation is already adopted for the fabrication of LSI devices. In the field of memory products, samples of 16K DRAM, high speed 1Kx1 H MOS RAM, 1Kx4 MOS SRAM have been developed one after another. Among them, the highest complexity has reached 40000 components/chip, the integration density being about 2000 components/mm^2.

1K SRAM's and 4K DRAM's have already been put into production. the former ones are fabricated with N channel silicon gate isoplanar technology. One type of these circuits is a 6 transistor cell, 128 x 8 bit, a single + 5 V supply and TTL compatible. It has a read/write cycle of 500 ns, and a maximum access time of 320 ns, power consumption of 500 mw. Another type of static 1K x 1 bit RAM employs Poly-Silicon loads and dynamic peripherals, its access time ≤200 ns, power consumption ≤40 mw.

The 4K DRAM uses single transistor cell. It has a maximum access time of 250 ns, a maximum cycle time of 450 ns, power consumption $\leq$500 mw (active) and $\leq$20 mw (standby).

A 4K static RAM built with N channel silicon gate MOS technology has a chip size of 3.6 x 5.77 mm^2, a integration density of 27000 components/chip. It employs a 6 transistor cell, access time $\leq$ 300 ns, power consumption being 525 mw. The phto of the chip is shown in Fig.1.

An 8K EPROM is fabricated by N channel ion implantation process with a double layer Poly-Silicon structure. Its memory cell is composed of single NMOS transistor,operating under 3 supplies, access time $<$450 ns. This device has already been put into production in some plants. Development work for 16 K single supply EPROM is also underway in some units.

The 16 K DRAM has a chip size of 3 x 5.85 mm^2, a complexity of 40346. Its chip structure shown in Fig.2. It uses a single transistor cell and 3 supplies, read/write cycle time being 500 ns, access time being 250 ns. The development for the single supply 16 K DRAM is underway.

In the sphere of bipolar LSI memories, ECL 1K RAM and TTL 1 K RAM have been developed. The ECL 1K RAM has a typical addres access time of 20 ns. The power consumption of TTL 1K RAM is below 650mw, access time $<$ 45 ns, write time $<$ 20 ns, chip area 4.05 x 3.25 mm^2. Various high speed low power consumption TTL digital logic devices are now in production, gradually forming families.

In the realm of microprocessors and microcomputers, some research units have developed the DJS-052 and the DJS-062 8 bit products.

DJS-052 microprocessor adcpts the " 6 μm design rule ". Its effective chip area is 4.3 x 4.9 mm^2. It is interchangable with 8080A produced by Intel. In conjunction with our home semiconductor memory devices and input/cutput devices, it can implement a basic microccmputer.

DJS-062 8 bit microcomputer (Fig.3) is compatible with MC6800 made by Motolora. This machine consists of single chip microprocessor (MPU), 1K static RAM's, electrically reprogrammable ultraviolet erasable 8K EPROM's, Peripheral Interface Adapters (PIA), Assynchronous Communication Interface Adapters (ACIA), and Synchronous Serial Interface Adapters (SSIA). Corresponding circuits have been made in China.

At present, microprocessors and microcomputers are gradually expanding their application in national economy and science-technology field.Mainly in automatic control and computer aided design facilities.

A 16 bit word length microcomputer 77-II has also been developed. The 16 bit microprocessor is composed of two LSI chips, one ALU and one PLA. These chips are fabricated with conventional N channel si-gate MOS process.

Research work for CCD imaging devices has been carried out in some units. 512 x 320 bit CCD Surface Array Image Sensors have been designed and developed. Solid state cameras have been assembled with such sensors, obtaining clear images (Fig.4) this device employs a tri-phase tri-layer Poly-Silicon electrode structure, N type surface channel, frame transfer read out. Chip area is 13.32 x 9.1 mm^2. Chip complexity is in the 164 K components level. Photo- sensitive area is 7.7 x 6.1 mm^2. Photo-sensitive cell has a size of 24 x 24 μm^2.

II Microfabrication Technology

Microfabrication technique is an indispensable basis for the development of LSI and VLSI. In recent years, major progress in this field is as follow.

Electron Beam Lithography

The DB-2 electron beam exposure system made in 1974, is the first experimental prototype applied to device studies and production in China. This equipment employs vector scanning mode, minimum beam spot being 0.3 μm, scanning area 1 x 1~2 x 2 mm^2. Fig.5 shows the electrode pattern portion of the type CD42(5GHz, 1w) transistor fabricated with the DB-2. The chip consists of 24 emitter stripes, 0.7 μm wide and 35 μm long. Due to the poor wide alignment accuracy of the DB-2 work table, however only composite masks can be fabricated. Type DB-3A E-beam exposure system developed recently utilizes a laser alignment system making the alignment accuracy of the work table reaching ± 0.5 μm Scanning area is 1x1~4x4 mm^2, minimum line width being 0.7 μm. This equipment has already been applied to the fabrication of masks for transistors and ICs, making masks for Ku band GaAs FET and bubble memories of several tens K bits.

Now raster scan E-beam exposure system with better alignment accuracy and higher scanning speed, and E-beam projection exposure systems are being developed.

Optical Projection Exposure System

Optical projectors can produce fine lines with high throughput. It's considered to be the desirable method for making lines

of 1~3 μm. Several research units in China have succeeded in developing a DSW (Direct Stepping on Wafer), projection exposure machine (the prototype system ZGK 50, Fig.6). Reduction rate achievable is 5:1. The project lens of 14 mm image field diameter has a resolution of 1.5 μm. Two off-axis automatic alignment methods have been tried, one being laser alignment, another wafer edge alignment with self- alignment accuracy better than ± 0.25 μm. The precision positioning of the work table is provided by the coded ruler and photo-electric microscope system giving an accuracy of ± 0.33 μm. This prototype is now on- line for trial production. It exposes 12 wafers of 2" every hour. 1:1 full reflection projection exposers are also under developed.

X – ray Lithography

With the aim of achieving sub-micron line width, work on 20kvA soft X-ray exposure equipment is going on in China. Poly- imide or silicon are used for mask material. High precision alignment technique and soft X-ray resists are under research in the laboratory stage.

Dry Etching Process

Dry etching process plays an important role in microfabrication. In our country, barrel type plasma etching equipment are widely used in various LSI and CCD device development and production. They are commonly used for the etching of Poly-Si, silicon nitride and the stripping photo resist.

Parallel plate electrode plasma etch are used for etching a variety of materials. Etching Al lines with CCl_4 and A_r gas has obtained submicron geometries with line width and spacings of

0.75 μm.

In processing multilayer metallization systems of Pt-W-Pt-Au and Pt-Mo-Pt-Au for Si MW devices, inert gas sputtering etch is frequently used for the etching of Pt and Au.

Ion beem etching is a new technique developed in the last few years. Recently, type LK-1 ion beam etching system is developed in China. Its structure is shown in Fig.7. The major features are: beam energy 150～1000 ev; continuously adjustable; effective beam spot diameter 70 mm; beam density deviation within the effective beam spot area $\leqslant \pm$ 5%. With an M6800 microcomputer controlling the precision motion of the work table, the set is capable of executing a "weighted etch", according to etch depth variation function. This etcher has met the stringent etch requirement for SAW devices, integrated optics, LSI, bubble devices, MW devices and infra-red devices. Thin narrow patterns of 0.8x280 μm^2 with uniform line width and sharp edge definitions have been obtained.

Ion Implantation

Since 1970, systems with various energy level (5～30 kev, 150kev, 400kev and 600kev) have been developed, thus, paving the way for introducing advanced ion implantation techniques into our research development and production. At present, ion implantation is already widely used in LSI, MW and optoelectronic device fabrications. Fig.8 shows a mltipurpose high energy implant system with a wide anergy level from 20 to 445kev. It can implant ions of a variety of elements with atomic mass under 140. The system has already been used in R & D of Si avalenche photo diodes, MW power transistors, wrist watch IC's, nuclear radiation detectors and GaAs

double heterojunction laser devices as well as GaAs MESFET's.

In addition to those mentioned above, the system has also been used to implant H^+ or Ar^+ into garnets for bubble device studies, implant N^+ into niobium, B^+ into iron, nickel and stainless, steel for the studies of super conductivity and modification of metal and alloy properties.

A600kev high energy ion implant system developed recently has an energy range from 80 to 600 kev, continuously adjustable.Mass resolution $m/\Delta m$ is 200, $\Delta m=1$. Beam intensities for O^+, Ar^+ and H^+ are all over 100μA, for B^+, P^+ over 30μA. The major features are:

(1) Asymmetrical electrostatic three-cylindrical lenses are used, providing simultaneous acceleration and focusing, thus increasing the energy of ions entering the analyzer and reducing energy dispersion, while matching the variation in voltage of the attractive electrode, enabling a wide range of adjustment.

(2) A double focusing magnetic analyzer with asymmetry between object distance and image distance at an angle of deflection of 90° is used, thus enabling the use of small, light magnet and improving resolution. The magnet used is of the vertical type.

(3) By using electro-static switch, it can either function as a neutral beem deflector or a multiple target, and may be installed with multiple targets, thus multi-purpose operation. This implanter has already been used in research works on many types of devices, such as O^+ implant for planar GaAs MESFET's, P^+ implant for buried channel Si CCD's as well B^+ implant for Si SIT's etc.

In our laboratories, an ion imaging implant equipment has also been developed. The accelerating voltage is 120 kv. Image reduction ratio is 7:1. Image size is 2x2 mm^2. Minimum realized line

width is 2 μm.

Laser Annealing

The mechanism of the laser annealing as well as its applications in device manufacture is currently under theoretical studies and experimental research. Laser annealing has already been used in eliminating the crystal lattice damage resulted from ion implant processing. The post-annealing impurity redistribution effect in implanted samples have been studied and experimentally determined.

Laser annealing has also been applied to the annealing of LPCVD and atmosphere pressure CVD poly-Si films etc. Studies were made on the crystal orientations, grain structures and the variations in their electrical property. An example includes the studies of 5000 Å LPCVD films (original grain size 200~400 Å) processed by a ruby laser. It was found that the grain size grew up to 0.5~1 μm. When B^+ and P^+ implanted Poly- Si layers were laser annealed, the activation ratio of their carriers increased up to near 100 %, When Poly-Si was exposed to YAG laser radiation at a high repetitive frequency, remarkable increase in grain size (generally larger than 2 μm) was observed. Some even grew up to 10 μm. High purity Ge films on N-type GaAs epitaxial layers were annealed by pulsed laser beams generated by a Q-switch Nd: YAG laser. Good ohmic contact was obtained. The best specific contact resistivity was as low as $1 \times 10^{-6} \Omega - cm^2$. Experimental results showed that the method of producing N-type GaAs ohmic contacts with laser alloyed Ge film is feasible process to GaAs device and IC production.

Thin and Ultra-thin Epitaxial layer Growth Processes

Several research units have succeeded in building molecular

beam epitaxy systems, which are now used in the studies of multi-layer epitaxy and the physical characteristics of epitaxial layers. Various vapor phase and liquid phase epitaxial processes are being widely used in device and IC R & D. The technique of using organo-metallic compounds of tri- methyl gallium (TMG) and arsine (AsH_3) in CVD (MO-CVD) has been used to grow GaAs epitaxial materials with superior quality.

multi-layer liquid phase epitaxial technique with In Ga As P/ In P has been successfully used in developing various long wave-length lasers with wavelengths of 1.1, 1.3 and 1.55 μm. The birth of these laser devices has opened the way to high capacity, long distance optical fibre communication.

III Work Done on IC R & D

HMOS devices are very impotant in the development of LSI and VLSI. R. H. Dennard et al proposed the theory of scaling rule in 1972. This has been the basic theory for short channel MOS device design. Several units in China have developed HMOS devices with channel length of $2\sim4$ μm. Experiments were made connecting effects of substrate resistivity, negative substrate bias and channel geometry on threshold voltage V_T. The characteristics and effective channel length (Leff) of a single transistor with channel length L=2 μm were measured. A high speed 1K E/D MOS SRAM(mentioned above) has been fabricated with a 3 μm channel length(effective channel length 2.4 μm) and gate oxide thickness of 700 Å and source- drain junction depth <0.5 μm. The performance gained is typical access time less than 40 ns (refer to Fig.9). The relationship between experimental values of the threshold voltage V_T

and the channel length under drain voltage of V_{DC} = 0.1 v is shown in Fig.1C. The experimental results can be expressed approximately by the commonly used equation:

$$V_T = V_{FB} + 2\phi_F + \frac{Q_B}{C_{OX}} \left[1 - \left(\sqrt{1 + \frac{2W}{X_J}} - 1 \right) \frac{X_J}{L} \right]$$

where V_{FB} = flatband voltage, ϕ_F= fermic potential, C_{CX} = gate oxide capacity per unit surface area, L = effective channel length, X_J = junction depth, W = width of depletion region beneath the center of the gate region.

At the same time, experimental studies and theoretical analyses in HMOS devices with channel length below 2 μm is being carried out.

With its inherent features of low power consumption and wide range of working voltage, CMOS devices are gaining more and more attention. Many types of Al gate CMOS devices are already in production in our plants in China, while memories, microprocessors, A/D and D/A converters are under development.

Some research units are now employing CCD and MOS devices for the development of high resolution colour TV imagers.

In the bipolar branch of IC technology, some units have proposed a designing theory for 1 μm and sub-micron bipolar IC's, and obtianed a structure and impurity distribution profile with poly-Si self-aligned technique which can meet the high speed, high density and low power consumption requirements of LSI's. Some workers have proposed and dveloped an Integrated Injection Schottky logic devices (I^2SL). This type of I^2SL devices merges four structures into one. It has vertical PNP transistor with a buried collector as its injector, merged with a downward operated NPN transistor. An isolated wall parasitic transistor is used as a non-saturated

lateral PNP device and the Schottky diodes are fabricated on the collector region of the NPN invertor. Experimental I^2SL devices made with 6～8 μm epitaxial layers and 8 μm minimum line width acquire a gate delay under 20 ns (5 times faster than the conventional I^2L). Some researchers have proposed and developed a new type of logics - it is called DYL in China. The basic functional unit is a linear " and - or " gate, constituted with a new type of double gain composite transistor. In conjunction with switching elements, they perform all the logic functions required by the system. The linear " and - or " gate is structurally simple. Fabricated with conventional processes, it easily achieves high speed (gate delays less than 1 ns). Recent work has shown that the DYL devices can be used to implement tri-state logic, thus providing an attractive approach to the implementation of multi-state logic systems.

GaAs IC is a new area in ICs. Several C～Ku band low noise GaAs MESFET (Fig.11) and power GaAs MESFET have been developed. Work is being done in the development of monolithic MW GaAs IC's, high and ultra high speed digital GaAs devices and C band monolithic MW amplifiers. A depletion type buffer FET logic (BFL) has a gate delay under 100 ps. 2.1P

Bubble memories and cryogenic super conductivity devices are also being researched.

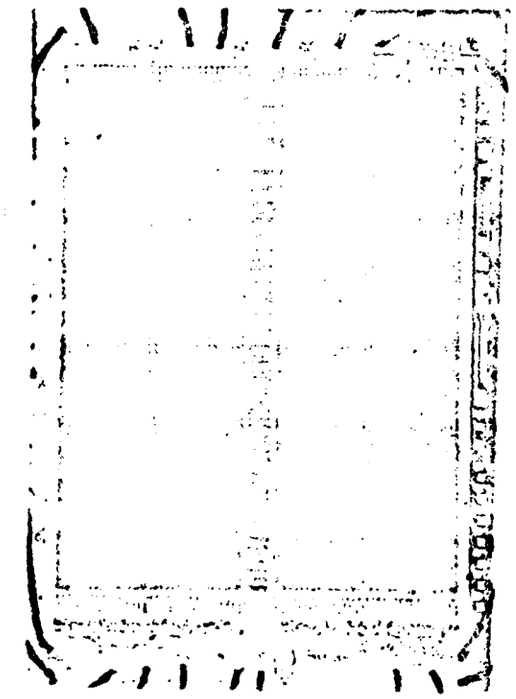

Fig.1. 4K static RAM chip.

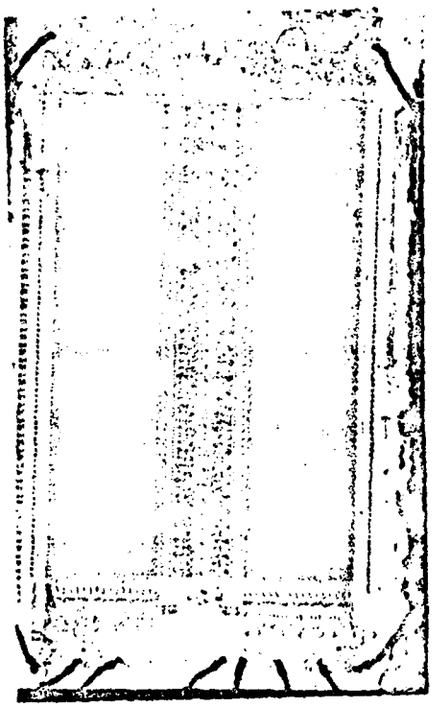

Fig.2. 16K DRAM chip.

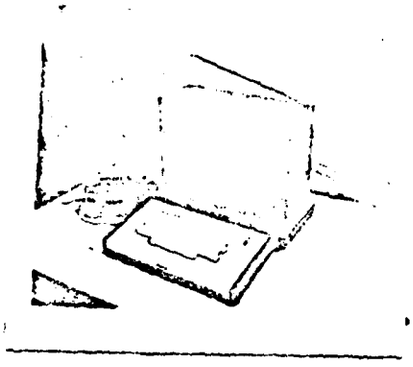

Fig.3. DJS-062 microcomputer.

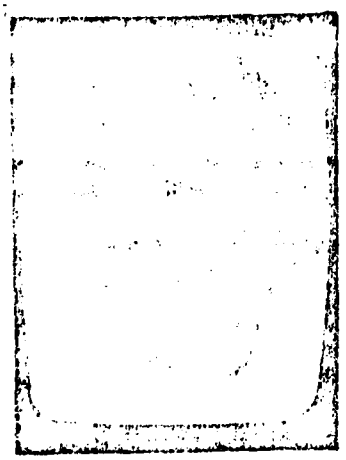

Fig.4. A clear image achieved by 512x320 CCD image sensor.

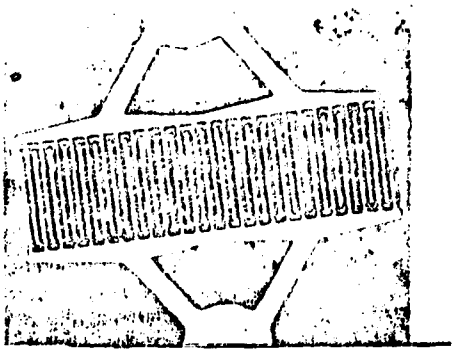

Fig.5.The electrode pattern portion of CD-42(5GHz,1W) transistor.

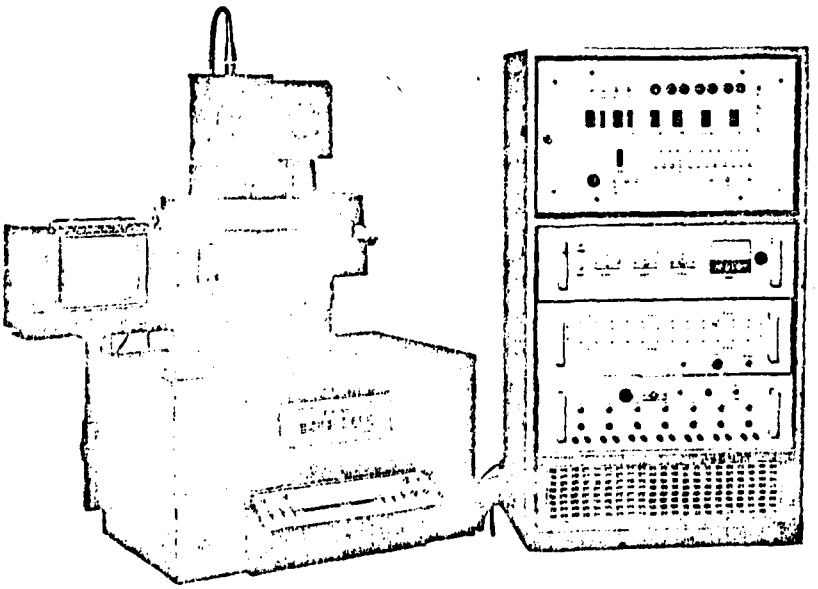

Fig. 6.The proto-type system ZGK-50.

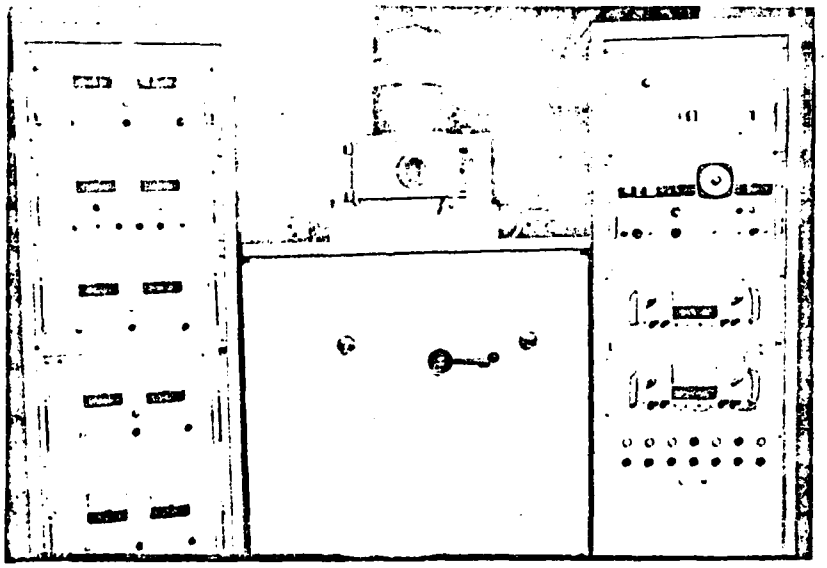

Fig.7. A type LK-1 ion beam etcher.

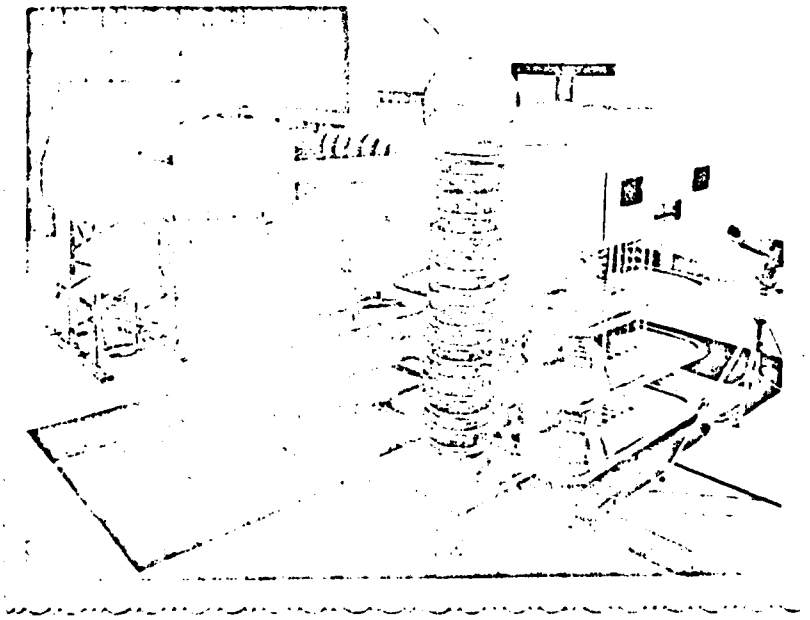

Fig. 8. A 20 to 445 Kev multi function high energy implant system.

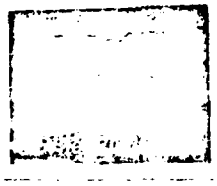

Fig.9. 1K bit HMOS RAM's access time.

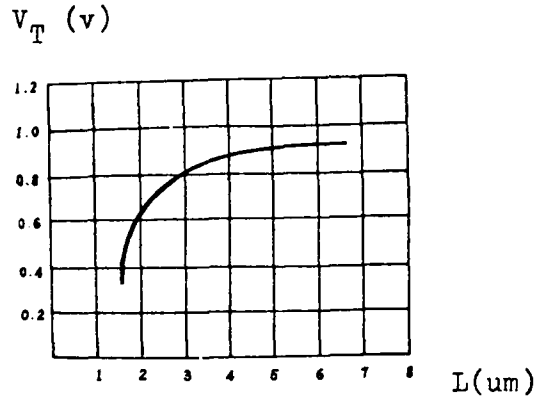

Fig.10. Threshold voltage versus channel length (V_{DS} = 0.10v, V_{BS}= -3.00v).

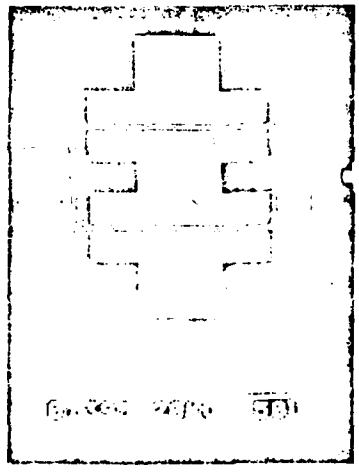

Fig.11. Low noise GaAs MESFET chip.

THOMSON-CSF
VISION COMPOSANTS MICROONDE

January 6th, 1982

A B S T R A C T

A R I - Microelectronics Symposium -

Circuit Configurations and limitations with new high-speed integrated circuit devices. Thomson- C.S.F. - D.C.M. - Domaine de Corbeville - ORSAY (France) - J. MAGARSHACK -

A survey will be given of different basic high speed integrated circuit structures using Si, GaAs and ternary compounds.

The state of the art performances of different logic gates will be given and commented (power, delay times, fan out dependance, etc ...) especially for micron and sub-micron device cells.

Basic analogue functions will also be revued and discussed ; amplifiers, oscillators, mixers, phase shifters, etc ... and a critical appraisal will be attempted of the different approaches.

Finally predictions and a discussion of the limitations will be undertaken in as fas as the basic module structure is concerned for increasing speed and reducing power and surface area.

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